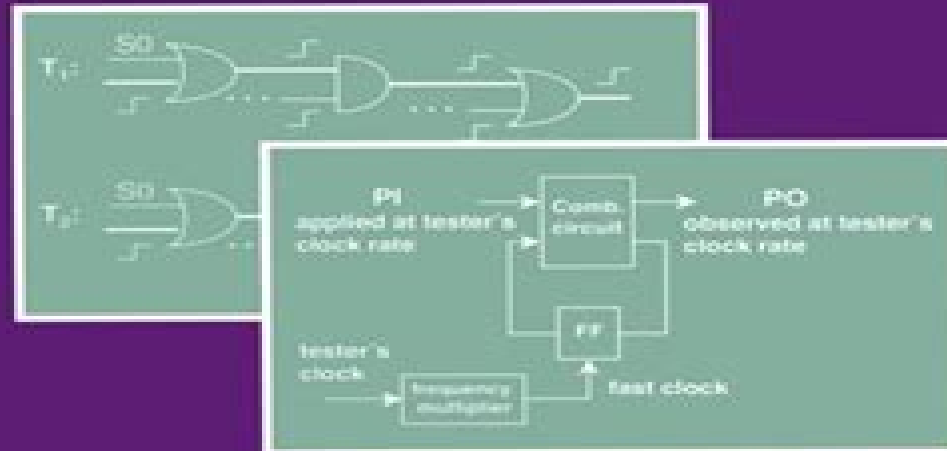


Delay Fault Testing for VLSI Circuits

Angela Krstić / Kwang-Ting (Tim) Cheng



Foreword by Vishwani D. Agrawal

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Delay Fault Testing For Vlsi Circuits

Angela Krstic, Kwang-Ting (Tim) Cheng

Delay Fault Testing For Vlsi Circuits:

Delay Fault Testing for VLSI Circuits Angela Krstic, Kwang-Ting (Tim) Cheng, 2012-12-06 In the early days of digital design we were concerned with the logical correctness of circuits We knew that if we slowed down the clock signal sufficiently the circuit would function correctly With improvements in the semiconductor process technology our expectations on speed have soared A frequently asked question in the last decade has been how fast can the clock run This puts significant demands on timing analysis and delay testing Fueled by the above events a tremendous growth has occurred in the research on delay testing Recent work includes fault models algorithms for test generation and fault simulation and methods for design and synthesis for testability The authors of this book Angela Krstic and Tim Cheng have personally contributed to this research Now they do an even greater service to the profession by collecting the work of a large number of researchers In addition to expounding such a great deal of information they have delivered it with utmost clarity To further the reader's understanding many key concepts are illustrated by simple examples The basic ideas of delay testing have reached a level of maturity that makes them suitable for practice In that sense this book is the best x DELAY FAULT TESTING FOR VLSI CIRCUITS available guide for an engineer designing or testing VLSI systems Tech niques for path delay testing and for use of slower test equipment to test high speed circuits are of particular interest **Path Delay Fault**

Testing for Digital VLSI Circuits Using Specialized Binary Decision Diagrams Kyriakos A. Christou, 2012 **Test Generation of Crosstalk Delay Faults in VLSI Circuits** S. Jayanthi, M.C. Bhuvaneshwari, 2018-09-20 This book describes a variety of test generation algorithms for testing crosstalk delay faults in VLSI circuits It introduces readers to the various crosstalk effects and describes both deterministic and simulation based methods for testing crosstalk delay faults The book begins with a focus on currently available crosstalk delay models test generation algorithms for delay faults and crosstalk delay faults before moving on to deterministic algorithms and simulation based algorithms used to test crosstalk delay faults Given its depth of coverage the book will be of interest to design engineers and researchers in the field of VLSI Testing

Models in Hardware Testing Hans-Joachim Wunderlich, 2009-11-12 Model based testing is the most powerful technique for testing hardware and software systems Models in Hardware Testing describes the use of models at all the levels of hardware testing The relevant fault models for nanoscaled CMOS technology are introduced and their implications on fault simulation automatic test pattern generation fault diagnosis memory testing and power aware testing are discussed Models and the corresponding algorithms are considered with respect to the most recent state of the art and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance **IEEE VLSI Test Symposium**, 2004 *Efficient Algorithms for Timing Verification and Delay Fault Testing* Liren Liu, 1991 *IDDQ Testing of VLSI Circuits* Ravi K. Gulati, Charles F. Hawkins, 1992-12-31 Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid 1970s Both Sandia Labs and RCA in the United States and

Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current IDDQ contained defects. Later this intuition was supported by data and analysis in the 1980s by Levi RACD Malaiya and Su SUNY Binghamton Soden and Hawkins Sandia Labs and the University of New Mexico Jacomino and co workers Laboratoire d Automatique de Grenoble and Maly and co workers Carnegie Mellon University. Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits in particular the complexity of finding suitable tests is very high. In comparison the IDDQ test does not observe the logic states but measures the integrated current that leaks through all gates. In other words it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages during the years that followed its initial announcements skepticism about the practicality of IDDQ testing prevailed. The idea however provided a great opportunity to researchers. New results on test generation fault simulation design for testability built in self test and diagnosis for this style of testing have since been reported. After a decade of research we are definitely closer to practice.

Tutorial, Test Generation for VLSI Circuits Sharad C. Seth, 1987 18th IEEE VLSI Test Symposium, 2000. Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems. Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques. Other subjects are analog test techniques temperature and process drift issues test compaction and design validation analog BIST and functional test and verification issues. Also covered are STIL extension IDDQ test and on line testing and fault tolerance. Lacks a subject index. Annotation copyrighted by Book News Inc Portland OR.

18th International Conference on VLSI Design International Conference on VLSI Design, 2005. **19th IEEE VLSI Test Symposium**, 2001. Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems. Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction. Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing. Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints. No subject index.

Book News Inc **Science Abstracts**, 1995 **Journal of Information Science and Engineering**, 2000

Proceedings of the ... European Test Conference ,1993 Proceedings ,1997 *Twelfth International Conference on VLSI Design* VLSI Society of India,IEEE Circuits and Systems Society,1999 The proceedings of the January 1999 conference consist of 103 papers 11 talks and six tutorials The papers are grouped under the headings of TCAD to ECAD low power testing co design and synthesis analog design multi valued logic verification digital signal processor DSP logic synthesis **Asian Test Symposium** ,2005 **Incremental Boolean Satisfiability and Its Application to Electronic Design Automation** Joonyoung Kim,2001 *Proceedings of the Third IEEE International Symposium on High Performance Distributed Computing* ,1994 The proceedings of HPDC 3 comprise three invited papers and 34 contributed papers in technical sessions devoted to software tools and environments high speed networks and applications HPDC applications mapping and scheduling distributed shared memory systems partitioning and load balancing *Applications of Artificial Intelligence in Engineering XI* Robert A. Adey,George Rzevski,A. K. Sunol,1996 Abstracts of papers presented at the Eleventh International Conference on the Applications of Artificial Intelligence in Engineering held at the Sheraton Sand Key Resort Clearwater Florida in September 1996

Decoding **Delay Fault Testing For Vlsi Circuits**: Revealing the Captivating Potential of Verbal Expression

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