

# Clock-CMOS (C<sup>2</sup>MOS)

- ❑ *Static CMOS*: the output of a static logic gate is valid so long as the input value are valid and the circuit has stabilized
- ❑ However, logic delays are due to the “rippling” through the circuits
  - » Not reference to any specific time base
  - » So on, Clock CMOS, or C<sup>2</sup>MOS is proposed
- ❑ C<sup>2</sup>MOS concept: non-overlapping clock

$$\phi(t) \cdot \bar{\phi}(t) = 0 \quad (9.9)$$

$$\Rightarrow \bar{\phi}(t) = V_{DD} - \phi(t) \quad (9.10)$$

- » But in physical signal, the clocks may overlap slightly during a transition

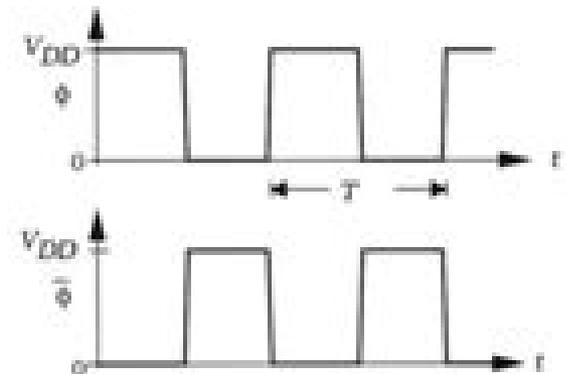


Figure 9.11 Clock signals

# C2mos Integrated Circuits Technical Data

**M Lipman**



## **C2mos Integrated Circuits Technical Data:**

## Unveiling the Magic of Words: A Report on "**C2mos Integrated Circuits Technical Data**"

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