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DESIGN



42nd Edition

# Computer Aided Design International Conference On Iccad 91

**Robert M. Fuhrer, Steven M. Nowick**



## **Computer Aided Design International Conference On Iccad 91:**

Language-driven Exploration and Implementation of Partially Re-configurable ASIPs Anupam Chattopadhyay, Rainer Leupers, Heinrich Meyr, Gerd Ascheid, 2008-12-02 Increasing complexity of modern embedded systems demands system designers to ramp up their design productivity without compromising performance goals This is promoted by modern Electronic System Level ESL techniques Language driven Exploration and Implementation of Partially Re configurable ASIPs addresses an important segment of the ESL area by modeling partially re configurable processors via high level Architecture Description Language ADL This approach also hints an imminent evolution in the area of re configurable system design

*Sequential Optimization of Asynchronous and Synchronous Finite-State Machines* Robert M. Fuhrer, Steven M. Nowick, 2012-12-06 Asynchronous or unclocked digital systems have several potential advantages over their synchronous counterparts In particular they address a number of challenging problems faced by the designers of large scale synchronous digital systems power consumption worst case timing constraints and engineering and design reuse issues associated with the use of a fixed rate global clock Moreover while for synchronous systems these problems are exacerbated by increasing system size asynchronous systems promise to scale more gracefully *Sequential Optimization of Asynchronous and Synchronous Finite State Machines Algorithms and Tools* makes three contributions to the field of sequential optimization for finite state machines 1 it introduces several new provably optimal algorithms for the synthesis and optimization of asynchronous finite state machines FSMs 2 it presents practical software implementations of each of these algorithms and 3 it introduces a complete new CAD package called MINIMALIST binding these tools into a state of the art technology independent synthesis path for burst mode asynchronous circuits Throughout this book real world industrial designs are used as benchmark circuits to validate the usefulness of the tools As an additional benefit some of the theory and tools also provide new methods for the optimization of synchronous FSMs

Binary Decision Diagrams and Applications for VLSI CAD Shin-ichi Minato, 1995-11-30 Symbolic Boolean manipulation using binary decision diagrams BDDs has been successfully applied to a wide variety of tasks particularly in very large scale integration VLSI computer aided design CAD The concept of decision graphs as an abstract representation of Boolean functions dates back to the early work by Lee and Akers In the last ten years BDDs have found widespread use as a concrete data structure for symbolic Boolean manipulation With BDDs functions can be constructed manipulated and compared by simple and efficient graph algorithms Since Boolean functions can represent not just digital circuit functions but also such mathematical domains as sets and relations a wide variety of CAD problems can be solved using BDDs *Binary Decision Diagrams and Applications for VLSI CAD* provides valuable information for both those who are new to BDDs as well as to long time aficionados from the Foreword by Randal E Bryant Over the past ten years BDDs have attracted the attention of many researchers because of their suitability for representing Boolean functions They are now widely used in many practical VLSI CAD systems this book can serve as an introduction to

BDD techniques and it presents several new ideas on BDDs and their applications many computer scientists and engineers will be interested in this book since Boolean function manipulation is a fundamental technique not only in digital system design but also in exploring various problems in computer science from the Preface by Shin ichi Minato

**Application-Driven Architecture Synthesis** Francky Catthoor, Lars-Gunnar Svensson, 2012-12-06 Application Driven Architecture Synthesis describes the state of the art of architectural synthesis for complex real time processing In order to deal with the stringent timing requirements and the intricacies of complex real time signal and data processing target architecture styles and target application domains have been adopted to make the synthesis approach feasible These approaches are also heavily application driven which is illustrated by many realistic demonstrations used as examples in the book The focus is on domains where application specific solutions are attractive such as significant parts of audio telecom instrumentation speech robotics medical and automotive processing image and video processing TV multi media radar sonar Application Driven Architecture Synthesis is of interest to both academics and senior design engineers and CAD managers in industry It provides an excellent overview of what capabilities to expect from future practical design tools and includes an extensive bibliography

**High-Level VLSI Synthesis** Raul Camposano, Wayne Wolf, 2012-12-06 The time has come for high level synthesis When research into synthesizing hardware from abstract program like descriptions started in the early 1970s there was no automated path from the register transfer design produced by high level synthesis to a complete hardware implementation As a result it was very difficult to measure the effectiveness of high level synthesis methods it was also hard to justify to users the need to automate architecture design when low level design had to be completed manually Today's more mature CAD techniques help close the gap between an automatically synthesized design and a manufacturable design Market pressures encourage designers to make use of any and all automated tools Layout synthesis logic synthesis and specialized datapath generators make it feasible to quickly implement a register transfer design in silicon leaving designers more time to consider architectural improvements As IC design becomes more automated customers are increasing their demands today's leading edge designers using logic synthesis systems are training themselves to be tomorrow's consumers of high level synthesis systems The need for very fast turnaround a competitive fabrication market WhlCh makes small quantity ASIC manufacturing possible and the ever growing complexity of the systems being designed all make higher level design automation inevitable

**The VLSI Handbook** Wai-Kai Chen, 2019-07-17 Over the years the fundamentals of VLSI technology have evolved to include a wide range of topics and a broad range of practices To encompass such a vast amount of knowledge The VLSI Handbook focuses on the key concepts models and equations that enable the electrical engineer to analyze design and predict the behavior of very large scale integrated circuits It provides the most up to date information on IC technology you can find Using frequent examples the Handbook stresses the fundamental theory behind professional applications Focusing not only on the traditional design methods it contains all relevant sources of information and tools to

assist you in performing your job This includes software databases standards seminars conferences and more The VLSI Handbook answers all your needs in one comprehensive volume at a level that will enlighten and refresh the knowledge of experienced engineers and educate the novice This one source reference keeps you current on new techniques and procedures and serves as a review for standard practice It will be your first choice when looking for a solution *Journal of Semicustom ICs*, 1991 *Index of Conference Proceedings* British Library. Document Supply Centre, 1994 □□□□□□□□□□ □□□□□□□□□□ □□□□□□□□□□ (Japan), 1900 **Memory-Based Logic Synthesis** Tsutomu Sasao, 2011-03-01 This book describes the synthesis of logic functions using memories It is useful to design field programmable gate arrays FPGAs that contain both small scale memories called look up tables LUTs and medium scale memories called embedded memories This is a valuable reference for both FPGA system designers and CAD tool developers concerned with logic synthesis for FPGAs

**Proceedings**, 1994 **Comp Euro**, 1992 *Proceedings of the International Conference on Application Specific Array Processors* José A. Fortes, Edward A. Lee, Teresa H. Meng, 1992 *Proceedings of the 35th Midwest Symposium on Circuits and Systems* Robert W. Newcomb, Bernard Geller, Mona Elwakkad Zaghloul, 1992 **Statistical Approach to VLSI** Stephen W. Director, W. Maly, 1994 This volume is the first complete overview of VLSI design methods that use statistical techniques for dealing with the random phenomena that are inherent in all VLSI manufacturing processes VLSI design today cannot be performed without taking into account economic related issues such as yield cost and performance oriented tradeoffs The book includes practical methods relevant to real life applications It contains edited papers by top industrial and academic specialists in the field These papers describe all three categories of CAD tools employed for statistical design IC performance optimization tools process simulation tools and tools for characterization of process fluctuations In each category both practical approaches and more theoretical approaches are presented **Rectangle Replacement and Variable Ordering** Søren Søren, 1994 *VLSI 91* Arne Halaas, Peter B. Denyer, 1992 The major problem in VLSI is really the control of complexity The hardest part is the control of autonomous yet interacting processes We do not yet have satisfactory techniques for handling that sort of thing but I think the techniques we need to develop are independent of whether you are programming or designing the chip Sidney Michaelson Initiator of the IFIP Working Group on VLSI This proceedings dedicated to the late Prof Sidney Michaelson who ten years ago established this IFIP Working Group reflects the continuing interest in improving design tools and the wide range of engineering concerns surrounding the effective exploitation of VLSI *International Test Conference, 1992* Institute of Electrical and Electronics Engineers, 1992 Annotation The proceedings of the 23rd edition of the premier technical conference on electronic testing held in Baltimore Maryland September 1992 comprise papers panels and tutorials in the areas of design and test integration test management software test hardware device assembly and system test and IEEE test standards ITC s 1992 theme Discover the New World of Test and Design reflects the growing emphasis on tighter integration of test and design to assure the highest quality products No subject index Ruggedly bound for heavy use

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