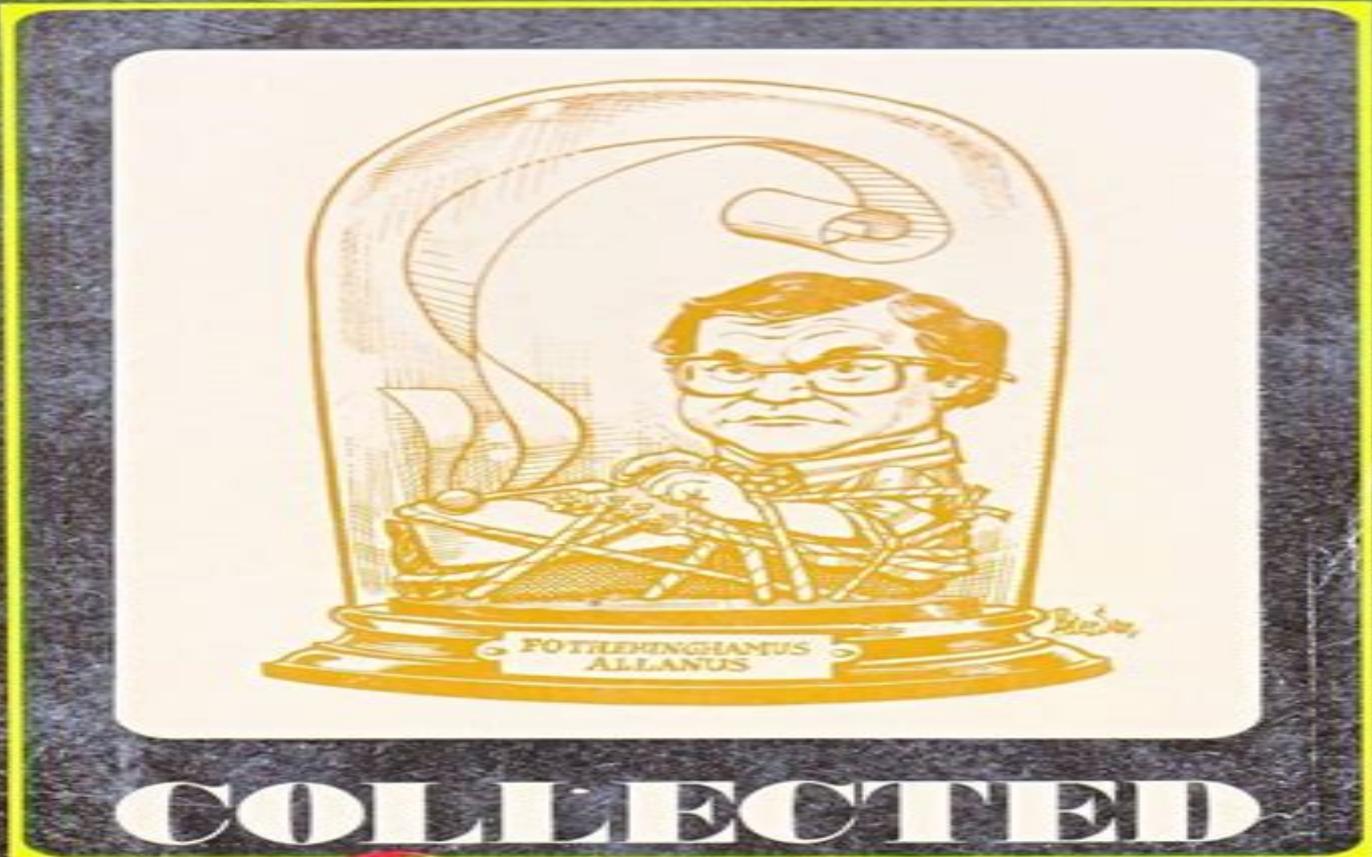


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web control of the i 2 c bus may be taken when the p bit is set or the bus is idle in firmware controlled master mode user

code conducts all i<sup>2</sup>c bus operations based on start and stop bit condition detection start and stop condition detection is  
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web bidirectional i<sup>2</sup>c stands for inter integrated circuit communications i<sup>2</sup>c is implemented in the picmicro by a hardware module called the master synchronous serial port known as the mssp module

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