

A Versatile Method for MOSFETs Commutations Analysis in Switching Power Converters Design

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Abstract - This paper discusses a novel method for the analysis of MOSFETs commutations and the investigation of related losses and spike current issues in Switching Power Converters (SPC) Design. The Synchronous Rectification Switching Cells (SRSC) configuration is considered for the investigation, which is used in High-Frequency High-Efficiency (H²EF) SPC design. The proposed method is aimed at providing an effective tool for quick feasibility investigations and comparative evaluations among design solutions using different MOSFETs combinations for the design of H²EF SPCs. The method allows to use non-linear models of inter-electrode MOSFETs capacitances and adopts a novel numerical technique specifically developed to solve the SRSC model ensuring robust and fast simulations. Capacitive pulsating currents circulating through the MOSFETs and the SPC during commutations can be analyzed in detail by using the proposed method. Some examples are presented to show how the specific characteristics of MOSFETs and the operating conditions influence as the switching losses as the pulsing currents circulating through the SPC.

Index Terms— MOSFETs commutations, parasitic capacitances, MOSFETs switching losses evaluation.

NOMENCLATURE

LS = Low Side; HS = High Side
 LSM = LS MOSFETHSM = HS MOSFET
 x = L or H subscript for LSM or HSM assignment
 V_{gs} [V] = gate voltage
 V_{gds} [V] = gate-drain voltage
 V_{gsv} [V] = gate-source voltage
 V_{ds} [V] = drain-source voltage
 V_{drv} [V] = driver voltage
 V_{th} [V] = threshold voltage
 V_{Tb} [V] = body-diode thermal voltage
 R_{gds} [Ω] = gate driver resistance
 R_{gsi} [Ω] = gate internal resistance
 I_{gs} [A] = gate current
 I_{chs} [A] = channel current
 I_{ds} [A] = drain-source current
 I_{sat} [A] = saturation current
 I_{bd} [A] = body-diode current

V_{in} [V] = input voltage
 R_{in} [Ω] = input line resistance
 I_{in} [A] = input current
 I_{o} [A] = output current average value
 β_n [A/V²] = transconductance
 λ_n [V⁻¹] = channel-length modulation
 I_{Cds} [A] = drain-source capacitance current
 I_{Cgd} [A] = gate-drain capacitance current
 I_{Cgs} [A] = gate-source capacitance current
 C_{ds} [F] = drain-source capacitance
 C_{gd} [F] = gate-drain capacitance
 C_{gs} [F] = gate-source capacitance
 C_{in} [F] = input capacitance
 C_{out} [F] = output capacitance
 C_{tr} [F] = transfer capacitance
 Q_{gs} [C] = gate-source charge
 Q_{gd} [C] = gate-drain charge
 Q_{ds} [C] = drain-source charge
 $x_{v_{ds}}$ = sign of voltage v_{ds} and voltage v_{ds}

I. INTRODUCTION

A wide variety of topologies and switching techniques and several types of power silicon devices are adopted for switch mode power supplies design. Nevertheless, most of high-efficiency power supplies for low-voltage high-current DC-DC applications, such as Point-of-Load (PoL) and Telecom (TLC) regulators, use couples of MOSFETs to form the Synchronous Rectification Switching Cell (SRSC) configurations, also defined as Half-Bridge Leg, shown in Figure 1. Due to their positions, the two MOSFETs are commonly labeled as High-Side (HS) MOSFET (Q_{hd}) and Low-Side (LS) MOSFET (Q_{ld}). Configurations (a) and (c) can be found in buck, boost and buck-boost converters and in primary side of active clamp Forward and Flyback converters. Configuration (b) can be found in self-driven secondary side of active clamp Forward converters. Depending on the specific topology, the voltage and current sources of Figure 1 may represent either real sources (e.g. battery) or passive energy storage devices (inductors, capacitors). The discussion of the model presented in this paper is referred to configuration (a), but it can be easily extended to other ones too.

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