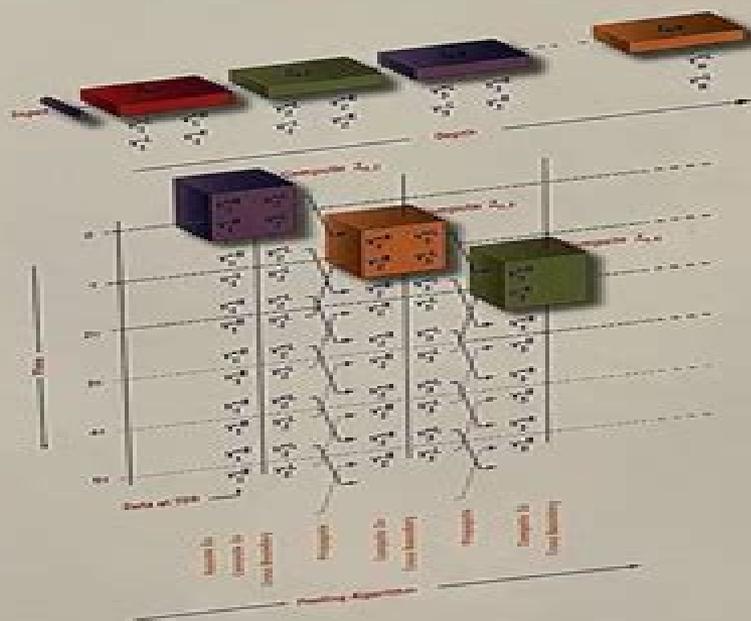


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David Pellerin, Scott Thibault



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Digital Signal Integrity Brian Young, 2001 Maximizing the performance of digital systems means optimizing their high speed interconnections Digital Signal Integrity gives engineers all the theory and practical methods they need to accurately model and simulate those interconnections and predict real world performance Whether you're modeling microprocessors memories DSPs or ASICs these techniques will get you to market faster with greater reliability

Power Integrity Modeling and Design for Semiconductors and Systems Madhavan Swaminathan, A. Ege Engin, 2008 Madhavan Swaminathan received his B E in Electronics and Communication from Regional Engineering College Tiruchirapalli in 1985 and his M S and Ph D degrees in Electrical Engineering from Syracuse University in 1989 and 1991 respectively He is currently the Joseph M Pettit Professor in Electronics in the School of Electrical and Computer Engineering and Deputy Director of the Packaging Research Center Georgia Tech He is also the cofounder of Jacket Micro Devices a company specializing in RF modules for wireless applications Prior to joining Georgia Tech he was with IBM where he worked on packaging for super computers His work on Power Integrity has won several awards and he was made an IEEE Fellow for his contributions in this area Ege Engin received his B S and M S degrees in electrical engineering from Middle East Technical University Ankara Turkey and from University of Paderborn Germany From 2001 to 2004 he was with the Fraunhofer Institute for Reliability and Microintegration in Berlin During this time he also received his Ph D from the University of Hannover Germany He is currently a Research Engineer in the School of Electrical and Computer Engineering and an Assistant Research Director of the Packaging Research Center at Georgia Tech He has more than 40 publications in refereed journals and conferences in the areas of signal and power integrity modeling and simulation

The First Comprehensive Example Rich Guide to Power Integrity Modeling Professionals need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems Now for the first time there's a complete guide to power integrity modeling everything you need to know from the basics through the state of the art Using realistic case studies and downloadable software examples two leading experts demonstrate today's best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise The authors carefully introduce the core concepts of power distribution design systematically present and compare leading techniques for modeling noise and link these techniques to specific applications Their many examples range from the simplest using analytical equations to compute power supply noise through complex system level applications The authors introduce power delivery network components analysis high frequency measurement and modeling requirements Thoroughly explain plane modeling including plane behavior lumped modeling distributed circuit based approaches and much more Offer in depth coverage of simultaneous switching noise including modeling for time and frequency domain analysis Introduce three leading time domain simulation methods rational function methods signal flow graphs and MNA Present these and other advanced case studies high speed

servers high speed differential signaling chip package analysis embedded decoupling capacitors and electromagnetic bandgap structures This book s system level focus and practical examples will make it indispensable for every professional concerned with power integrity including electrical engineers system designers signal integrity engineers and materials scientists It will also be valuable to developers building software that takes advantage of high speed systems During my M S undergraduate days in a little town called Tiruchirapalli in Southern India we used to have frequent voltage and current surges that knocked out all the electrical equipment such as fans and lights in our rooms Frustrated my friend once remarked We are Powerless to solve the Current problem Of course he meant this in jest but little did I realize that this would become the theme of my research for many years Though my area is on Semiconductors and computer system

Compact Models and Measurement Techniques for High-Speed Interconnects Rohit Sharma, Tapas

Chakravarty, 2012-02-17 Compact Models and Measurement Techniques for High Speed Interconnects provides detailed analysis of issues related to high speed interconnects from the perspective of modeling approaches and measurement techniques Particular focus is laid on the unified approach variational method combined with the transverse transmission line technique to develop efficient compact models for planar interconnects This book will give a qualitative summary of the various reported modeling techniques and approaches and will help researchers and graduate students with deeper insights into interconnect models in particular and interconnect in general Time domain and frequency domain measurement techniques and simulation methodology are also explained in this book

Noise Coupling in System-on-Chip Thomas Noulis, 2018-01-09 Noise Coupling is the root cause of the majority of Systems on Chip SoC product fails The book discusses a breakthrough substrate coupling analysis flow and modelling toolset addressing the needs of the design community The flow provides capability to analyze noise components propagating through the substrate the parasitic interconnects and the package Using this book the reader can analyze and avoid complex noise coupling that degrades RF and mixed signal design performance while reducing the need for conservative design practices With chapters written by leading international experts in the field novel methodologies are provided to identify noise coupling in silicon It additionally features case studies that can be found in any modern CMOS SoC product for mobile communications automotive applications and readout front ends

Modeling and Design of Electromagnetic Compatibility for High-Speed Printed Circuit Boards and Packaging Xing-Chang Wei, 2017-09-19 Modeling and Design of Electromagnetic Compatibility for High Speed Printed Circuit Boards and Packaging presents the electromagnetic modelling and design of three major electromagnetic compatibility EMC issues related to the high speed printed circuit board PCB and electronic packages signal integrity SI power integrity PI and electromagnetic interference EMI The emphasis is put on two essential passive components of PCBs and packages the power distribution network and the signal distribution network This book includes two parts Part one talks about the field circuit hybrid methods used for the EMC modeling including the modal method the integral equation method

the cylindrical wave expansion method and the de embedding method Part two illustrates EMC design methods and explores the applications of novel metamaterials and two dimensional materials on traditional EMC problems This book is designed to enhance worthwhile electromagnetic theory and mathematical methods for practical engineers and to train students with advanced EMC applications

Practical FPGA Programming in C David Pellerin, Scott Thibault, 2005 FPGA brings high performance applications to market quickly this book covers the many emerging platforms in a proven effective manner

High-speed Interconnect Design and Characterization Pingshan Wang, 2004 **High-speed Interconnect Design, Characterization, and Applications** Jinsook Kim, 2006 Simulation and Modeling Techniques for Signal Integrity and Electromagnetic Interference on High Frequency Electronic Systems Luca Daniel, 2003 High-Speed Signaling Kyung Suk (Dan) Oh, Xing Chao (Chuck) Yuan, 2011-10-07 New System Level Techniques for Optimizing Signal Power Integrity in High Speed Interfaces from Pioneering Innovators at Rambus Stanford Berkeley and MIT As data communication rates accelerate well into the multi gigahertz range ensuring signal integrity both on and off chip has become crucial Signal integrity can no longer be addressed solely through improvements in package or board level design Diverse engineering teams must work together closely from the earliest design stages to identify the best system level solutions In High Speed Signaling several of the field s most respected practitioners and researchers introduce cutting edge modeling simulation and optimization techniques for meeting this challenge Edited by pioneering experts Drs Dan Oh and Chuck Yuan these contributors explain why noise and jitter are no longer separable demonstrate how to model their increasingly complex interactions and thoroughly introduce a new simulation methodology for predicting link level performance with unprecedented accuracy The authors address signal integrity from architecture through high volume production thoroughly discussing design implementation and verification Coverage includes New advances in passive channel modeling power supply noise and jitter modeling and system margin prediction Methodologies for balancing system voltage and timing budgets to improve system robustness in high volume manufacturing Practical stable formulae for converting key network parameters Improved solutions for difficult problems in the broadband modeling of interconnects Equalization techniques for optimizing channel performance Important new insights into the relationships between jitter and clocking topologies New on chip measurement techniques for in situ link performance testing Trends and future directions in signal integrity engineering High Speed Signaling thoroughly introduces new techniques pioneered at Rambus and other leading high tech companies and universities approaches that have never before been presented with this much practical detail It will be invaluable to everyone concerned with signal integrity including signal and power integrity engineers high speed I O circuit designers and system level board design engineers

SOC (System-on-a-Chip) Testing for Plug and Play Test Automation Krishnendu Chakrabarty, 2002-09-30 Various aspects of system on a chip SOC integrated circuit testing are addressed in 13 papers on test planning access and scheduling test data compression and interconnect crosstalk and signal integrity Topics

include concurrent test of core based SOC design and testing for interconnect crosstalk defects using on chip embedded processor cores The editor is affiliated with Duke University The book is reprinted from a Special Issue of the Journal of Electronic Testing vol 18 nos 4 5 There is no subject index Annotation c 2003 Book News Inc Portland OR booknews com

Advanced Electronic Packaging Richard K. Ulrich, William D. Brown, 2006-02-24 As in the First Edition each chapter in this new Second Edition is authored by one or more acknowledged experts and then carefully edited to ensure a consistent level of quality and approach throughout There are new chapters on passive devices RF and microwave packaging electronic package assembly and cost evaluation and assembly while organic and ceramic substrates are now covered in separate chapters All the hallmarks of the First Edition which became an industry standard and a popular graduate level textbook have been retained An Instructor s Manual presenting detailed solutions to all the problems in the book is available upon request from the Wiley Marketing Department *Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation* Johan Vounckx, Nadine Azemard, 2006-09-08 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41 revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more *Electrical Performance of Electronic Packaging*, 2004 Symposium Record, 2002 *Electrical Modeling of Packaging, Interconnects, and Logic for High Speed Computer Design* David E. O'Brien, 1993 *Proceedings of the International Conference on Electromagnetic Interference and Compatibility*, 2003 *International Symposium on Quality Electronic Design*, 2002 Annotation Fifty one papers and 21 posters from the March 2002 symposium report current research in deep submicron integrated circuit design and development The sessions address interconnect extraction and modeling design for process variations metrics power and noise management verification signal integrity and low power design techniques Some of the topics are transition aware global signaling TAGS the interoperability of EDA tools for sequential logic synthesis statistical methods for the determination of process corners power supply noise suppression via clock skew scheduling and the relation between SAT and BDDs for equivalence checking No subject index Annotation copyrighted by Book News Inc Portland OR

Microelectronic Interconnects and Packages, 1991 Fourth International Symposium on Quality Electronic Design, 2003 ISQED looks into the research development and application of design techniques and methods design processes and EDA design methodologies and tools that address issues that impact the quality of the realization of designs into physical integrated circuits It emphasizes a holistic approach toward design quality and to highlight and accelerate cooperation among the IC Design EDA Semiconductor Process Technology and Manufacturing communities

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