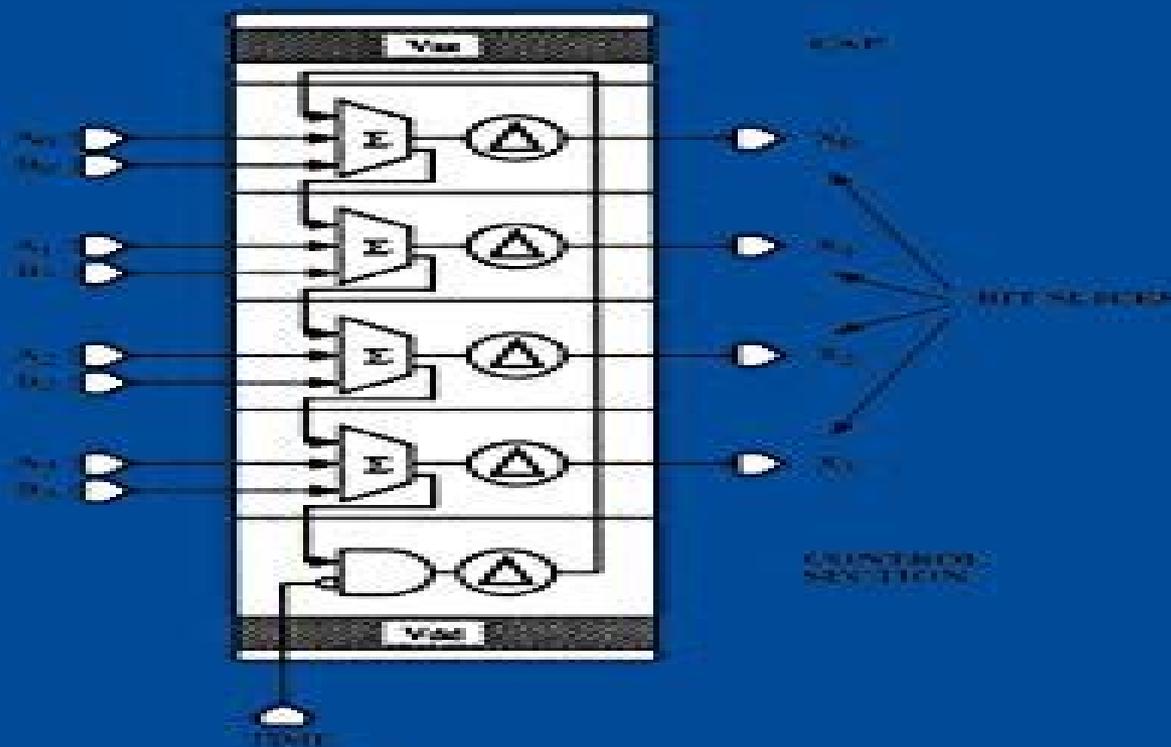


# DIGIT-SERIAL COMPUTATION

Richard I. Hartley  
Keshab K. Parhi



# Digit Serial Computation

**Antonio Laganà, Marina L.  
Gavrilova, Vipin Kumar, Youngsong  
Mun, C.J. Kenneth Tan, Osvaldo Gervasi**

## **Digit Serial Computation:**

*Digit-Serial Computation* Richard Hartley, Keshab K. Parhi, 2012-12-06 Digital signal processing DSP is used in a wide range of applications such as speech telephone mobile radio video radar and sonar The sample rate requirements of these applications range from 10 KHz to 100 MHz Real time implementation of these systems requires design of hardware which can process signal samples as these are received from the source as opposed to storing them in buffers and processing them in batch mode Efficient implementation of real time hardware for DSP applications requires study of families of architectures and implementation styles out of which an appropriate architecture can be selected for a specified application To this end the digit serial implementation style is proposed as an appropriate design methodology for cases where bit serial systems cannot meet the sample rate requirements and bit parallel systems require excessive hardware The number of bits processed in a clock cycle is referred to as the digit size The hardware complexity and the achievable sample rate increase with increase in the digit size As special cases a digit serial system is reduced to bit serial or bit parallel when the digit size is selected to equal one or the word length respectively A family of implementations can be obtained by changing the digit size parameter thus permitting an optimal trade off between throughput and size Because of their structured architecture digit serial designs lend themselves to automatic compilation from algorithmic descriptions An implementation of this design methodology the Parsifal silicon compiler was developed at the General Electric Corporate Research and Development laboratory

*Digit-Serial Computation* Richard Hartley, Keshab Parhi, 2012-10-12 Digital signal processing DSP is used in a wide range of applications such as speech telephone mobile radio video radar and sonar The sample rate requirements of these applications range from 10 KHz to 100 MHz Real time implementation of these systems requires design of hardware which can process signal samples as these are received from the source as opposed to storing them in buffers and processing them in batch mode Efficient implementation of real time hardware for DSP applications requires study of families of architectures and implementation styles out of which an appropriate architecture can be selected for a specified application To this end the digit serial implementation style is proposed as an appropriate design methodology for cases where bit serial systems cannot meet the sample rate requirements and bit parallel systems require excessive hardware The number of bits processed in a clock cycle is referred to as the digit size The hardware complexity and the achievable sample rate increase with increase in the digit size As special cases a digit serial system is reduced to bit serial or bit parallel when the digit size is selected to equal one or the word length respectively A family of implementations can be obtained by changing the digit size parameter thus permitting an optimal trade off between throughput and size Because of their structured architecture digit serial designs lend themselves to automatic compilation from algorithmic descriptions An implementation of this design methodology the Parsifal silicon compiler was developed at the General Electric Corporate Research and Development laboratory

*Floating-point On-line Arithmetic for Highly Concurrent Digit-serial Computation* Osaaki Watanuki, 1981

**J.UCS The Journal of Universal Computer Science** Hermann Maurer,Christian Calude,Arto Salomaa,2012-12-06 J UCS is the electronic journal that covers all areas of computer science The high quality of all accepted papers is ensured by a strict review process and an international editorial board of distinguished computer scientists The online journal J UCS is a prototype for modern electronic publishing Distributed via the Internet it supports all the search and navigation tools of advanced online systems This first annual print and CD ROM archive edition contains all articles published online in J UCS during 1995 It allows easy and durable access without logging onto the Internet Uniform citation of papers is guaranteed by identical page numbering and layout of all versions J UCS is based on HyperWave formerly Hyper G a networked hypermedia information system compatible with other systems *Digital Signal Processing for Multimedia Systems* Keshab K. Parhi,Takao Nishitami,2018-10-03 Addresses a wide selection of multimedia applications programmable and custom architectures for the implementations of multimedia systems and arithmetic architectures and design methodologies The book covers recent applications of digital signal processing algorithms in multimedia presents high speed and low priority binary and finite field arithmetic architectures details VHDL based implementation approaches and more

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materials techniques and examples in grating design and Maxwell equations in a truncated Fourier space *Genetic and Evolutionary Computing* Jeng-Shyang Pan, Pavel Krömer, Václav Snášel, 2013-08-04 Genetic and Evolutionary Computing This volume of Advances in Intelligent Systems and Computing contains accepted papers presented at ICGEC 2013 the 7th International Conference on Genetic and Evolutionary Computing The conference this year was technically co sponsored by The Waseda University in Japan Kaohsiung University of Applied Science in Taiwan and VSB Technical University of Ostrava ICGEC 2013 was held in Prague Czech Republic Prague is one of the most beautiful cities in the world whose magical atmosphere has been shaped over ten centuries Places of the greatest tourist interest are on the Royal Route running from the Powder Tower through Celetna Street to Old Town Square then across Charles Bridge through the Lesser Town up to the Hradcany Castle One should not miss the Jewish Town and the National Gallery with its fine collection of Czech Gothic art collection of old European art and a beautiful collection of French art The conference was intended as an international forum for the researchers and professionals in all areas of genetic and evolutionary computing The main topics of ICGEC 2013 included Intelligent Computing Evolutionary Computing Genetic Computing and Grid Computing 1992 ICO Topical Meeting on Optical Computing Andreï Markovich Goncharenko, 1993 **Genetic and Evolutionary Computing** Thi Thi Zin, Jerry Chun-Wei Lin, Jeng-Shyang Pan, Pyke Tin, Mitsuhiro Yokota, 2015-09-03 This volume of Advances in Intelligent Systems and Computing contains accepted papers presented at ICGEC 2015 the 9th International Conference on Genetic and Evolutionary Computing The conference this year was technically co sponsored by Ministry of Science and Technology Myanmar University of Computer Studies Yangon University of Miyazaki in Japan Kaohsiung University of Applied Science in Taiwan Fujian University of Technology in China and VSB Technical University of Ostrava ICGEC 2015 is held from 26 28 August 2015 in Yangon Myanmar Yangon the most multiethnic and cosmopolitan city in Myanmar is the main gateway to the country Despite being the commercial capital of Myanmar Yangon is a city engulfed by its rich history and culture an integration of ancient traditions and spiritual heritage The stunning SHWEDAGON Pagoda is the center piece of Yangon city which itself is famous for the best British colonial era architecture Of particular interest in many shops of Bogyoke Aung San Market and of world renown are Myanmar s precious stones rubies sapphires and jade At night time Chinatown comes alive with its pungent aromas and delicious street food The conference is intended as an international forum for the researchers and professionals in all areas of genetic and evolutionary computing Complex Digital Circuits Jean-Pierre Deschamps, Elena Valderrama, Lluís Terés, 2019-03-14 This textbook is designed for a second course on digital systems focused on the design of digital circuits It was originally designed to accompany a MOOC Massive Open Online Course created at the Autonomous University of Barcelona UAB currently available on the Coursera platform Readers will learn to develop complex digital circuits starting from a functional specification will know the design alternatives that a development engineer can choose to reach the specified circuit performance and will understand which design tools are available to

develop a new circuit     **IEEE Workshop on Signal Processing Systems** ,1998     *IEEE Symposium on FPGAs for Custom Computing Machines* Kenneth L. Pocek,Jeffrey M. Arnold,1996 Contains papers from the April 1996 symposium reporting on research in device architectures applications compilers and related software support Topics include using MORRPH in an industrial machine vision system a software development system for FPGA based data acquisition systems a reconfigura     Official Gazette of the United States Patent Office USA Patent Office,1915     *Decimal Computation* Hermann Schmid,1983     *Systolic Array Processors* J. V. McCanny,John McWhirter,Earl E. Swartzlander,1989

**Advanced Signal-processing Algorithms, Architectures, and Implementations** ,1993     **Field-programmable Logic and Applications** ,2002     Introduction to Digital Computer Engineering University of Michigan. Engineering Summer Conferences,1958 Vol for 1962 includes the preliminary edition of An introduction to digital computing by Bruce W Arden published in 1962 by the Addison Wesley Pub Co     *Proceedings of the ... Midwest Symposium on Circuits and Systems* ,1996

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