

A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders

Arash Ardakani and Mahdi Shabany

Abstract—Long-term evolution (LTE) is aimed to achieve the peak data rates in excess of 300 Mb/s for the next-generation wireless communication systems. Turbo codes, the specified channel-coding scheme in LTE, suffer from a low-decoding throughput due to its iterative decoding algorithms. One efficient approach to achieve a promising throughput is to use multiple maximum a posteriori (MAP) cores in parallel, resulting in a large area overhead. The two computationally challenging units in an MAP core are α and β recursion units. Although several methods have been proposed to shorten the critical path of these recursion units, their area-efficient architecture with minimum silicon area is still missing. In this brief, a novel relation existing between the α and β metrics is introduced, leading to a novel add-compare-select (ACS) architecture. The proposed technique can be applied to both the precise approximation of log-MAP and max-log-MAP ACS architectures. The proposed ACS design, which is implemented in a 6.13- μm CMOS technology and customized for the LTE standard, results in, at most, 18.1% less area compared with the reported designs to date while maintaining the same throughput level.

Index Terms—Add-compare-select (ACS) unit, long-term evolution (LTE), parallel architecture, radix-4, recursion unit, turbo decoder, very-large-scale integration (VLSI).

I. INTRODUCTION

MANY advanced wireless communication standards adopted turbo codes as the channel coding scheme due to its near Shannon error-correcting performance [1]. The decoding procedure is performed in two different half iterations, where the reliability of received bits is computed in the form of extrinsic values using interleavers and soft-input-soft-output (SISO) decoders in an iterative way. On even half iterations, the decoding process is performed on the noninterleaved data and parity, whereas on odd half iterations, the interleaved data are decoded. The extrinsic values, representing the reliability of the information bits, are sent to another half iteration by passing through the interleaver/deinterleaver unit until the acceptable error level is achieved.

Recently, long-term evolution (LTE) advanced has been dominated as the next-generation wireless communication standard, which is aimed at higher peak data rates close to 3 Gb/s [2]. The turbo decoder, which is specified in LTE, reveals to be a limiting block toward this goal due to its

iterative decoding nature, high latency, and significant silicon area consumption. The decoding procedure is performed using the algorithm presented in [3]. Since the implementation of the actual maximum a posteriori (MAP) algorithm incurs very high computational complexity, typically, two modified forms of the MAP algorithm, i.e., the max-log-MAP and log-MAP algorithms [4], [5], are commonly realized instead.

In these two alternative methods, the MAP core consists of log-likelihood ratio (LLR) units, as well as the core units to compute α , β , and γ , i.e., the forward, backward, and branch metrics, respectively. In fact, the α and β units, due to their recursive computation nature, are the most challenging units to implement, occupying almost 40% of the whole MAP core area [6]. The γ unit, on the other hand, is a trivial part of the turbo decoder, consisting of few addition computations. Therefore, an area-efficient architecture for α and β metrics computation is highly desirable, which has always been a challenge in literature.

In order to address this challenge, in this brief, a new relation between the α and β metrics is introduced; based on this new relation, a novel add-compare-select (ACS) unit for forward and backward computation is proposed. The proposed scheme results in, at most, an 18.1% reduction in the silicon area compared with the designs reported to date.

II. TURBO DECODER ALGORITHM

The MAP algorithm, which provides the *a posteriori* probability for each bit, is used in iterative decoding of turbo codes. The MAP algorithm provides the probability of the decoded bit u_k being either +1 or -1 for the received symbol sequence y by calculation of the LLR values as

$$L(u_k|y) = \log \left[\frac{p(u_k = +1|y)}{p(u_k = -1|y)} \right] \quad (1)$$

where $p(u_k = +1|y)$ and $p(u_k = -1|y)$ denote the probabilities of bit u_k being +1 and -1, respectively.

The turbo decoder specified in LTE consists of two recursive convolutional encoders, i.e., an interleaver and a feed-through path, as shown in Fig. 1(a). The feed-through passes one block of K information bits, which are called systematic bits x_k^s , where $k = 0, 1, \dots, K-1$. The parity generated by the convolutional encoder is denoted by x_k^p . By permuting the systematic bits via the interleaver, the second sequence of parity is generated by passing through the second convolutional encoder, which is denoted by $x_k^{p'}$. On the receiver side, the reliability of bits is computed iteratively by exchanging the extrinsic LLRs between two SISO decoders based on (1), as

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