

Defect and Fault Tolerance in VLSI Systems

Edited by
Israel Koren

Defect And Fault Tolerance In Vlsi Systems 2001

AN Whitehead



Defect And Fault Tolerance In Vlsi Systems 2001:

2001 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems ,2001 This volume features the proceedings of the International Symposium on Defect and Fault Tolerance in VLSI Systems DFT 2001 *Defect and Fault Tolerance in VLSI Systems* Israel Koren,2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized *Defect and Fault Tolerance in VLSI Systems* ,1988 Defect and Fault Tolerance in VLSI Systems C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher circuit densities increasingly more complex application objectives and advanced packaging technologies have substantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliability The emphasis on this area has resulted in a new field of interdisciplinary scientific research In fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturability and productivity of integrated circuit chips VLSI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should be continued preferably on a yearly basis It was Dr I Koren who organized the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were published as the first volume of this series 21 **Defect and Fault Tolerance in Vlsi Systems (dft 2002), 17th Ieee International Symposium** Ieee International Symposium On Defect And Fault Tolerance In Vlsi Systems,2002 **Proceedings** ,2005 *Defect and Fault Tolerance in VLSI Systems, IEEE International Symposium on* , Soft Errors in Modern Electronic Systems Michael

Nicolaidis,2010-09-24 This book provides a comprehensive presentation of the most advanced research results and technological developments enabling understanding qualifying and mitigating the soft errors effect in advanced electronics including the fundamental physical mechanisms of radiation induced soft errors the various steps that lead to a system failure the modelling and simulation of soft error at various levels including physical electrical netlist event driven RTL and system level modelling and simulation hardware fault injection accelerated radiation testing and natural environment testing soft error oriented test structures process level device level cell level circuit level architectural level software level and system level soft error mitigation techniques The book contains a comprehensive presentation of most recent advances on understanding qualifying and mitigating the soft error effect in advanced electronic systems presented by academia and industry experts in reliability fault tolerance EDA processor SoC and system design and in particular experts from industries that have faced the soft error impact in terms of product reliability and related business issues and were in the forefront of the countermeasures taken by these companies at multiple levels in order to mitigate the soft error effects at a cost acceptable for commercial products In a fast moving field where the impact on ground level electronics is very recent and its severity is steadily increasing at each new process node impacting one after another various industry sectors as an example the Automotive Electronics Council comes to publish qualification requirements on soft errors research and technology developments and industrial practices have evolve very fast outdated the most recent books edited at 2004 **Design and Test Technology for Dependable Systems-on-Chip** Ubar, Raimund,Raik, Jaan,Vierhaus, Heinrich Theodor,2010-12-31

This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC 2001 International Workshop on System-Level Interconnect Prediction ,2001 The SLIP workshop is a forum for the exchange of ideas at the interface between interconnect technology and physical design This year in recognition of the highly diverse backgrounds and motivations of the attendees SLIP 2001 has been organized around three mini tutorials a review of wire distribution models a look under the hood of a variety of system level interconnect modeling programs and back end of line yield modeling These tutorials set the scene for the paper sessions that follow Forward

Dependable Systems and Networks (DSN 2001) (Formerly FTCS) IEEE Computer Society,IEEE,PR&&&&,2001 Proceedings of a July 2001 conference covering all aspects of dependability in classical and networked computer systems as well as topical areas in IT There is a special focus on safety and security issues in embedded multimedia and Internet applications Papers are in sections on modeling algorithms software demos replication software robustness survivability and security wireless and mobile communications real time testing and runtime error detection models for fault tolerance hardware architecture and design group oriented systems and practical experiences Specific topics include model based synthesis of fault trees from MATLAB a dynamic replica selection algorithm for tolerating timing faults constructing self

testable software components and intrusion tolerant group management in enclaves This volume lacks a subject index c Book News Inc

Handbook of Algorithms for Physical Design Automation Charles J. Alpert, Dinesh P. Mehta, Sachin S. Sapatnekar, 2008-11-12 The physical design flow of any project depends upon the size of the design the technology the number of designers the clock frequency and the time to do the design As technology advances and design styles change physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in

19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2004-01-01 DFT 2004 showcases the latest research results in the in the field of defect and fault tolerance in VLSI systems Its papers cover yield defect and fault tolerance error correction and circuit system reliability and dependability *EH-2001* Didier Keymeulen, 2001 These proceedings contain 32 papers from the July 2001 conference in Long Beach the abstract of one invited talk is also included The focus of this year's workshop was to provide a roadmap from the current proof of concept stage of Evolvable Hardware to the development of larger scale real world systems addressing issues such as evolvability and scalability from the Preface Papers concentrate on topics like the relationships between biology and robotics the evolution of analog and mixed signal circuits survivable and flexible hardware the evolution of digital functions the evolution of signal processing circuits reconfiguration architecture and devices the evolution of CA brain inspired architecture evolvability and applications Author index only c Book News Inc

20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'05), Monterey, California, 03.10-05.10.2005, 20?? **Defect and Fault Tolerance in VLSI Systems**, 1998

2000 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2000 This work constitutes the proceedings of the 2000 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems DFT 2000 Subjects addressed include yield analysis and modelling wafer scale large area systems fault tolerant systems testing strategies and more

18th International Conference on VLSI Design International Conference on VLSI Design, 2005

Special Section on Defect and Fault Tolerance in VLSI Systems Way Kuo, Institute of Electrical and Electronics Engineers, 2003

[SOC \(System-on-a-Chip\) Testing for Plug and Play Test Automation](#) Krishnendu Chakrabarty, 2002-09-30 Various aspects of system on a chip SOC integrated circuit testing are addressed in 13 papers on test planning access and scheduling test data compression and interconnect crosstalk and signal integrity Topics include concurrent test of core based SOC design and testing for interconnect crosstalk defects using on chip embedded processor cores The editor is affiliated with Duke University The book is reprinted from a Special Issue of the Journal of Electronic Testing vol 18 nos 4 5 There is no subject index Annotation c 2003 Book News Inc Portland OR booknews.com

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