

## Components of System Bus



# Computer Architecture Complexity And Correctness

**S Ben Porath**



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**Computer Architecture** Silvia M. Mueller, Wolfgang J. Paul, 2013-11-11 Computer Architecture Complexity and Correctness develops at the gate level the complete design of a pipelined RISC processor with delayed branch forwarding hardware interlock precise maskable nested interrupts caches and a fully IEEE compliant floating point unit In contrast to other design approaches applied in practice and unlike other textbooks available the design presented here are modular clean and complete up to the construction of entire complex machines The authors systematically basing their approach on rigorous mathematical formalisms allows for rigorous correctness proofs accurate hardware costs determination and performance evaluation as well as generally speaking for coverage of a broad variety of relevant issues within a reasonable number of pages The book is written as a text for classes on computer architecture and related topics and will serve as a valuable source of reference for professionals in hardware design

**Computer Architecture: Complexity And**

**Correctness** Mueller, 2009-08-01 Correct Hardware Design and Verification Methods Daniel Geist, Enrico

Tronci, 2003-10-22 This book constitutes the refereed proceedings of the 12th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2003 held in L'Aquila Italy in October 2003 The 24 revised full papers and 8 short papers presented were carefully reviewed and selected from 65 submissions The papers are organized in topical sections on software verification automata based methods processor verification specification methods theorem proving bounded model checking and model checking and applications

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**and Verification Methods** Tiziana Margaria, Tom F. Melham, 2001-08-27 This book constitutes the refereed proceedings of the 11th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2001 held in Livingston Scotland UK in September 2001 The 28 revised full papers and eight short papers presented together with two invited papers and one special paper were carefully reviewed and selected from 56 submissions The book offers topical sections on model checking clocking issues theorem proving with higher order logics hardware compilation tools component verification case studies algorithm verification and duration calculus

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Barnard, David B. Skillicorn, 1988      *SIAM Journal on Computing* Society for Industrial and Applied Mathematics, 1997  
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