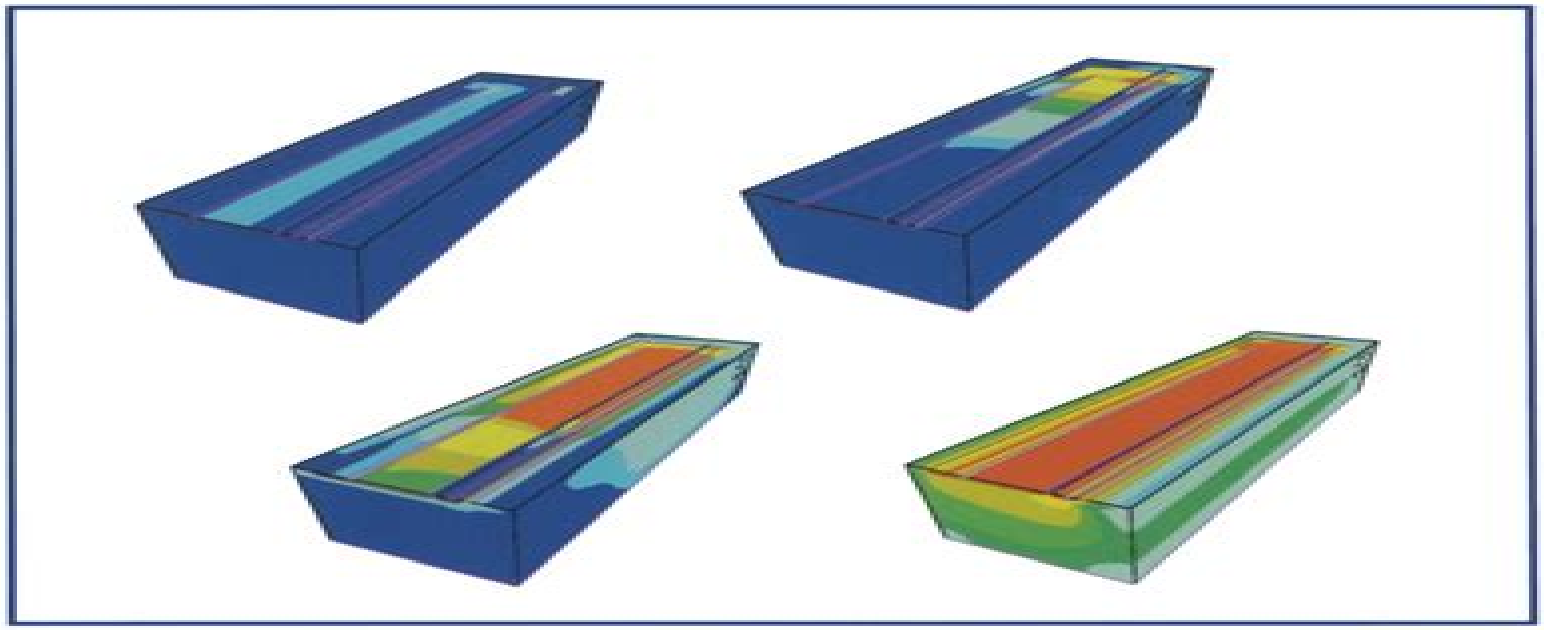
Advanced Simulation Methods for ESD Protection Development



Kai Esmark, Harald Gossner & Wolfgang Stadler

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E. Ajith Amerasekera,Charvaka Duvvury

Advanced Simulation Methods For Esd Protection Development:

ESD Protection Methodologies Marise Bafleur,Fabrice Caignet,Nicolas Nolhier,2017-07-26 Failures caused by electrostatic discharges ESD constitute a major problem concerning the reliability and robustness of integrated circuits and electronic systems This book summarizes the many diverse methodologies aimed at ESD protection and shows through a number of concrete studies that the best approach in terms of robustness and cost effectiveness consists of implementing a global strategy of ESD protection ESD Protection Methodologies begins by exploring the various normalized test techniques that are used to qualify ESD robustness as well as characterization and defect localization methods aimed at implementing corrective measures Due to the increasing complexity of integrated circuits it is important to be able to provide a simulation in which the implemented ESD protection strategy provides the desired protection while not harming the performance levels of the circuit Therefore the main features and difficulties related to the different types of simulation finite element SPICE type and behavioral are then studied To conclude several case studies are presented which provide real life examples of the approaches explained in the previous chapters and validate a number of the strategies from component to system level Provides a global ESD protection approach from component to system including both the proposal of investigation techniques and predictive simulation methodologies Addresses circuit and system designers as well as failure analysis engineers Provides the description of specifically developed investigation techniques and the application of the proposed methodologies to real case studies *System Level ESD Protection* Vladislav Vashchenko,Mirko Scholz,2014-03-21 This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge ESD protection It is an invaluable reference for anyone developing systems on chip SoC and systems on package SoP integrated with system level ESD protection The book focuses on both the design of semiconductor integrated circuit IC components with embedded on chip system level protection and IC system co design The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits thereby reducing or completely eliminating the need for additional discrete components on the printed circuit board PCB and meeting system level ESD requirements The authors take a systematic approach based on IC system ESD protection co design A detailed description of the available IC level ESD testing methods is provided together with a discussion of the correlation between IC level and system level ESD testing methods The IC level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing The overall methodology for IC system ESD co design is presented as a step by step procedure that involves both ESD testing and numerical simulations Advances in Solid State Circuit Technologies Paul Chu,2010-04-01 This book brings together contributions from experts in the fields to describe the current status of important topics in solid state circuit technologies It consists of 20 chapters which are grouped under the following categories general information circuits and devices materials and characterization techniques These chapters have been written by renowned

experts in the respective fields making this book valuable to the integrated circuits and materials science communities It is intended for a diverse readership including electrical engineers and material scientists in the industry and academic institutions Readers will be able to familiarize themselves with the latest technologies in the various fields **The ESD Handbook** Steven H. Voldman,2021-04-12 A practical and comprehensive reference that explores Electrostatic Discharge ESD in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection Written by a noted expert on the topic the text offers a topic by topic reference that includes illustrative figures discussions and drawings The handbook covers a wide range of topics including ESD in manufacturing garments wrist straps and shoes ESD Testing ESD device physics ESD semiconductor process effects ESD failure mechanisms ESD circuits in different technologies CMOS Bipolar etc ESD circuit types Pin Power Pin to Pin etc and much more In addition the text includes a glossary index tables illustrations and a variety of case studies Contains a well organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians operators engineers circuit designers and failure analysis engineers The ESD Handbook contains an accessible reference to ESD design and ESD systems ESD Steven H. Voldman,2011-04-04 Electrostatic discharge ESD continues to impact semiconductor components and systems as technologies scale from micro to nano electronics This book studies electrical overstress ESD and latchup from a whole chip ESD design synthesis approach It provides a clear insight into the integration of ESD protection networks from a generalist perspective followed by examples in specific technologies circuits and chips Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks are covered from a top down design approach Look inside for extensive coverage on integration of cores power bussing and signal pins in DRAM SRAM CMOS image processing chips microprocessors analog products RF components and how the integration influences ESD design and integration architecturing of mixed voltage mixed signal to RF design for ESD analysis floorplanning for peripheral and core I O designs and the implications on ESD and latchup guard ring integration for both a bottom up and top down methodology addressing I O guard rings ESD guard rings I O to I O and I O to core classification of ESD power clamps and ESD signal pin circuitry and how to make the correct choice for a given semiconductor chip examples of ESD design for the state of the art technologies discussed including CMOS BiCMOS silicon on insulator SOI bipolar technology high voltage CMOS HVCMOS RF CMOS and smart power practical methods for the understanding of ESD circuit power distribution ground rule development internal bus distribution current path analysis quality metrics ESD Design and Synthesis is a continuation of the author s series of books

on ESD protection It is an essential reference for ESD circuit and semiconductor engineers design synthesis team leaders layout design characterisation floorplanning test and reliability engineers technicians and groundrule and test site developers in the manufacturing and design of semiconductor chips It is also useful for graduate and undergraduate students in electrical engineering semiconductor sciences and manufacturing sciences and on courses involving the design of ESD devices chips and systems This book offers a useful insight into the issues that confront modern technology as we enter the nano electronic era **Simulation Methods for ESD Protection Development** Harald Gossner,Kai Esmark,Wolfgang Stadler,2003-10-16 Simulation Methods for ESD Protection Development looks at the integration of new techniques into a comprehensive development flow which is now available due advances made in the field during the recent years These findings allow for an early stable ESD concept at a very early stage of the technology development which is essential now development cycles have been reduced The book also offers ways of increasing the optimization and control of the technology concerning performance thus making the process more cost effective and increasingly efficient This title provides a guide through the latest research and technology presenting the ESD protection development methodology This is based on a combination of process device and circuit stimulation and addresses the optimization of the industry critical issue reduced development cycles Written to address the needs of the ESD engineer this text is required reading by all industry practitioners and researchers and students within this field The FIRST Extensive overview on the subject of ESD simulation Addresses the industry critical issue of reduced development cycles and provides solutions Presents the latest research in the field with high practical relevance and its results **ESD Basics** Steven H. Voldman,2012-10-22 Electrostatic discharge ESD continues to impact semiconductor manufacturing semiconductor components and systems as technologies scale from micro to nano electronics This book introduces the fundamentals of ESD electrical overstress EOS electromagnetic interference EMI electromagnetic compatibility EMC and latchup as well as provides a coherent overview of the semiconductor manufacturing environment and the final system assembly It provides an illuminating look into the integration of ESD protection networks followed by examples in specific technologies circuits and chips The text is unique in covering semiconductor chip manufacturing issues ESD semiconductor chip design and system problems confronted today as well as the future of ESD phenomena and nano technology Look inside for extensive coverage on The fundamentals of electrostatics triboelectric charging and how they relate to present day manufacturing environments of micro electronics to nano technology Semiconductor manufacturing handling and auditing processing to avoid ESD failures ESD EOS EMI EMC and latchup semiconductor component and system level testing to demonstrate product resilience from human body model HBM transmission line pulse TLP charged device model CDM human metal model HMM cable discharge events CDE to system level IEC 61000 4 2 tests ESD on chip design and process manufacturing practices and solutions to improve ESD semiconductor chip solutions also practical off chip ESD protection and system level solutions to provide more robust

systems System level concerns in servers laptops disk drives cell phones digital cameras hand held devices automobiles and space applications Examples of ESD design for state of the art technologies including CMOS BiCMOS SOI bipolar technology high voltage CMOS HVCMOS RF CMOS smart power magnetic recording technology micro machines MEMs to nano structures ESD Basics From Semiconductor Manufacturing to Product Use complements the author s series of books on ESD protection For those new to the field it is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano electronic Era **Silicon Germanium** Raminderpal Singh,Modest M. Oprysko,David Harame,2004-03-01 An excellent introduction to the SiGe BiCMOS technology from the underlying device physics to current applications Ron Wilson EETimes SiGe technology has demonstrated the ability to provide excellent high performance characteristics with very low noise at high power gain and with excellent linearity This book is a comprehensive review of the technology and of the design methods that go with it Alberto Sangiovanni Vincentelli Professor University of California Berkeley Cofounder Chief Technology Officer Member of Board Cadence Design Systems Inc Filled with in depth insights and expert advice Silicon Germanium covers all the key aspects of this technology and its applications Beginning with a brief introduction to and historical perspective of IBM s SiGe technology this comprehensive guide quickly moves on to Detail many of IBM s SiGe technology development programs Explore IBM s approach to device modeling and characterization including predictive TCAD modeling Discuss IBM s design automation and signal integrity knowledge and implementation methodologies Illustrate design applications in a variety of IBM s SiGe technologies Highlight details of highly integrated SiGe BiCMOS system on chip SOC design Written for RF analog and mixed signal designers CAD designers semiconductor students and foundry process engineers worldwide Silicon Germanium provides detailed insight into the modeling and design automation requirements for leading edge RF analog and mixed signal products and illustrates in depth applications that can be implemented using IBM s advanced SiGe process technologies and design kits This volume provides an excellent introduction to the SiGe BiCMOS technology from the underlying device physics to current applications But just as important is the window the text provides into the infrastructure the process development device modeling and tool development Ron Wilson Silicon Engineering Editor EETimes This book chronicles the development of SiGe in detail provides an in depth look at the modeling and design automation requirements for making advanced applications using SiGe possible and illustrates such applications as implemented using IBM s process technologies and design methods John Kelly Senior Vice President and Group Executive Technology Group IBM **Proceedings** ,2005 *Electrical Overstress/Electrostatic Discharge Symposium Proceedings* ,2004 **ESD in Silicon Integrated Circuits** E. Ajith Amerasekera,Charvaka Duvvury,2002-05-22 Examines the various methods available for circuit protection including coverage of the newly developed ESD circuit protection schemes for VLSI circuits Provides guidance on the implementation of circuit protection measures Includes new sections on ESD design rules layout approaches package effects and circuit concepts Reviews the new Charged Device Model

CDM test method and evaluates design requirements necessary for circuit protection **The British National Bibliography** Arthur James Wells,2004 **American Book Publishing Record** ,2004 *IBM Journal of Research and Development* ,2003 Proceedings, ... International Symposium on VLSI Design ,2003 *IEEE 2000 First International Symposium on Quality Electronic Design* ,2000 The Summary of Engineering Research University of Illinois (Urbana-Champaign campus). Engineering Experiment Station,University of Illinois (Urbana-Champaign campus). Office of Engineering Publications,1995 **Electrical & Electronics Abstracts** ,1997 **Proceedings of the IEEE 1999 Custom Integrated Circuits Conference** ,1999 **International Journal of Nanotechnology** ,2005

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